IN THE SPECIFICATION

Please amend the specification as indicated below.

Please insert the following header and paragraph at page 1, before the Background of the Invention section.

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. Patent Application Serial No. 10/306,627, filed November 26, 2002, which was a continuation of U.S. Patent Application Serial No. 09/566,069, filed May 5, 2000, now U.S. Patent No. 6,515,356, issued on February 4, 2003.

Please amend the paragraph beginning on page 6, line 26 as follows:

The present invention also provides a method for fabricating a semiconductor ~~packag~~ package. One embodiment within the present invention includes the steps of: providing a circuit board having a plurality of bond fingers and ball lands, the circuit board having a through hole formed at the center thereof; locating a semiconductor chip having a plurality of input/output pads at one face thereof in the through hole of the circuit board; electrically connecting the input/output pads of the semiconductor chip to the bond fingers of the circuit board through an electrical conductor such as bond wires; encapsulating the semiconductor chip, conductors, and a predetermined region of the circuit board with an encapsulant; and fusing conductive balls to the ball lands of the circuit board, to form input/output terminals.

Please amend the paragraph beginning on page 17, line 21 as follows:

Referring to FIG. 6, a predetermined circuit pattern layer can be formed on second face 11b of resin film 11 (BT epoxy resin film), as well as on first face 11a thereof. Specifically, first face 11a of resin film 11 has the circuit pattern layer composed of bond fingers 12, connection parts 13 and ball lands 15 formed thereon, and second face 11b also has a circuit pattern layer including connection parts 13 formed thereon. Here, the circuit pattern layers formed on first face 11a and second face 11b of resin film can be connected to

each other through a conductive via hole 14. Moreover, cover coat 16 can be additionally selectively coated on the circuit pattern layer formed on second face 11b of resin film 11 to protect it from external environments. In this embodiment, a layer of cover coat 16 is coated on second face 11b of resin film 11, second face 2b of semiconductor chip 2 and the top side of encapsulant 20. As shown in FIG. 6A, two semiconductor chips 2, 3 can be included back to back, with bond wires 6 attached respectively to the first or second circuit patterns.

Please amend the paragraph beginning on page 8, line 8 as follows.

Referring to FIG. 7, a plurality of ball lands 15 may be additionally formed at connection parts 13 of the circuit pattern layer formed on second face 11b of resin film 11. In this case, similar to the case of FIG. 6, the circuit pattern layer formed on first face 11a of resin film 11 and the circuit pattern layer formed on its second face 11b can be connected to each other through conductive via hole 14. Ball lands 15 are exposed out of cover coat 16, meaning that plural semiconductor packages can.be subsequently laminated. Conductive balls 30 of another package may be adhesively fused to the ball lands 15 formed on second face 11b of resin film 11, enabling a vertical stacking and electrical interconnection of the semiconductor packages, as shown in FIG. 7A.

Please amend the paragraph beginning on page 20, line 17 as follows:

Finally, as shown in FIG. 10G, when closing means C is a tape or ultraviolet tape, heat or ultraviolet light is irradiated on the top face of circuit board 10 to enable a removal (e.g., peeling) of closing means C, thereby externally exposing the top face of semiconductor chip 2. Where closing means a C is formed from a metal thin film, closing means C may be left in place. Furthermore, closing means C may be removed before conductive balls 30 are fused to ball lands 15 of circuit board 10, which is optional in the present invention.

Please amend the paragraph beginning on page 20, line 26 as follows:

FIGs. 11A and 11B are a plan view and a bottom view respectively, of a circuit board strip 100 for making semiconductor packages in accordance with the present invention. Referring to FIGs. 11A and 11B, a plurality of interconnected rectangular resin films 11, each

of which is perforated with a rectangular through hole 18, and each of which has four peripheral sides adjacent to each of which is a through slot 19, are arranged in the form of matrix, equally spaced apart, at a predetermined distance, to constitute one substrip 110. The semiconductor chip (not shown) will be placed in each through hole 18 of substrip 110. A plurality of substrips 110 are horizontally connected, with a vertically-perforated slot 111 having a predetermined length therebetween, to form one main strip 115.

Please amend the paragraph beginning on page 22, line 13 as follows:

FIGs. 11C and 11D are bottom views illustrating a state in which a cover lay tape 120, as closing means C, adheres to circuit board strip 100. Cover lay tape 120 is attached to the bottom side of circuit board strip 100. Referring to FIG. 11C, cover lay tape 120 adheres to the bottom of each substrip 110. That is, a piece of cover lay tape 120 can be attached to the bottom of each substrip 110. Although it is, of course, possible to employ a cover lay tape 120 with the same size as that of main strip 115, using cover lay tapes 120 each sized to ~~attache~~ attach to one face of each substrip 110 reduces a difference in the thermal expansion coefficients of the circuit board strip and cover lay tape, which increases with the length.